Abstracts

Pulse Regeneration in the Gigabit-Per-Second Range Using a Diode Differential Regenerator

U. Barabas. "Pulse Regeneration in the Gigabit-Per-Second Range Using a Diode Differential Regenerator." 1980 Transactions on Microwave Theory and Techniques 28.3 (Mar. 1980 [T-MTT]): 161-171.

A clocked pulse regenerator circuit (diode differential regenerator (DDR)) is described which employs a modified hybrid tee, step recovery diodes, and bipolar transistors. For the first time a hybrid tee is used in ultra broad-band digital applications. Signal pulses with bit rates up into the gigabit-per-second range are regenerated, the shape of the input pulses having no direct influence on the shape of the output pulses. Only the charge of the input signals determines the amplitudes of the output pulses. At a signal bit rate of 1 Gbit/s an insertion voltage gain of 20 dB was obtained. Operating the DDR in a push-pull mode the voltage gain is doubled to 26 dB. Because the output pulses of the DDR are very narrow the circuit can be used in time-division multiplexers providing output pulse streams with bit rates up to 16 Gbit/s and amplitudes of several volts across a load of 50 Omega. The internal behavior of the DDR is analyzed, among other things by the results of computer simulations. Calculations for optimizing the employed components are given.

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